Announcements

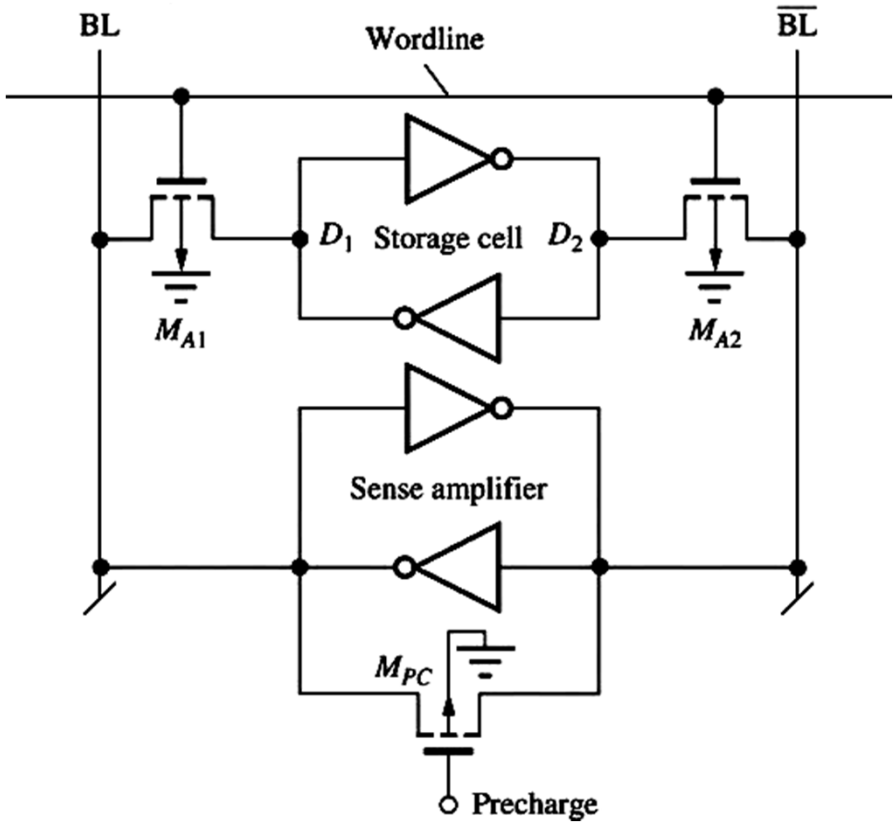
- (Crude) notes for switching speed example from lecture last week posted.
- Schedule Final Project demo with TAs.
- Written project report to include written evaluation section.
- Send me suggestions for review/example topics.

Sense Amplifiers

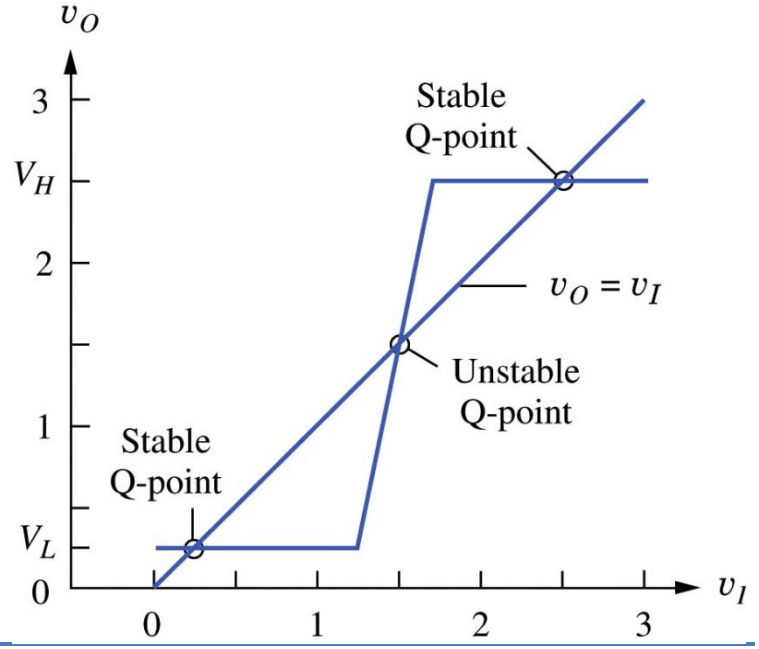
- Sense amplifiers are used to detect the small currents that flow through the access transistors or the small voltage differences that occur during charge sharing

Sense Amplifiers

6-T Cell



- M_{PC} is the precharge transistor whose purpose is to force the latch to operate at the unstable point.



Sense Amplifiers

6-T Cell Example

- For the figure on the previous slide, find the currents in the latch transistors when M_{PC} is turned on under the following conditions:

$$V_{DD} = 3\ V \qquad \left(\frac{W}{L}\right)_{All} = \frac{2}{1}$$

$NMOS$:	$PMOS$:
$K_n^{'} = 60\ \mu A/V^2$	$K_p^{'} = 25\ \mu A/V^2$
$V_{TO} = 0.7\ V$	$V_{TO} = -0.7\,V$
$\gamma = 0.5\ V^{1/2}$	$\gamma = 0.7\,V^{1/2}$
$2\phi_F = 0.6V$	$2\phi_F = 0.6\,V$

Sense Amplifiers

6-T Cell Example

- Since the output voltage should equal on both sides of the latch when M_{PC} is on, it is known that $V_{GS} = V_{DS}$ for the latch NMOS devices and $V_{SG} = V_{SD}$ for the latch PMOS devices. Therefore these transistors are saturated.
- Due to the symmetry of the situation, the drain currents must be equal giving the following:

$$\frac{K_p'}{2}\left(\frac{W}{L}\right)\left(V_{SG}+V_{TP}\right)^2 = \frac{K_n'}{2}\left(\frac{W}{L}\right)\left(V_{GS}-V_{TN}\right)^2$$

$$\frac{1}{2}\left(\frac{25\mu A}{V^2}\right)\left(\frac{2}{1}\right)\left(3-V_O-0.7\right)^2 = \frac{1}{2}\left(\frac{60\mu A}{V^2}\right)\left(\frac{2}{1}\right)\left(V_O-0.7\right)^2$$

$$35V_O^2 + 31V_O - 102.9 = 0 \rightarrow V_O = 1.33V$$

Sense Amplifiers

6-T Cell Example

- The drain currents are then found by:

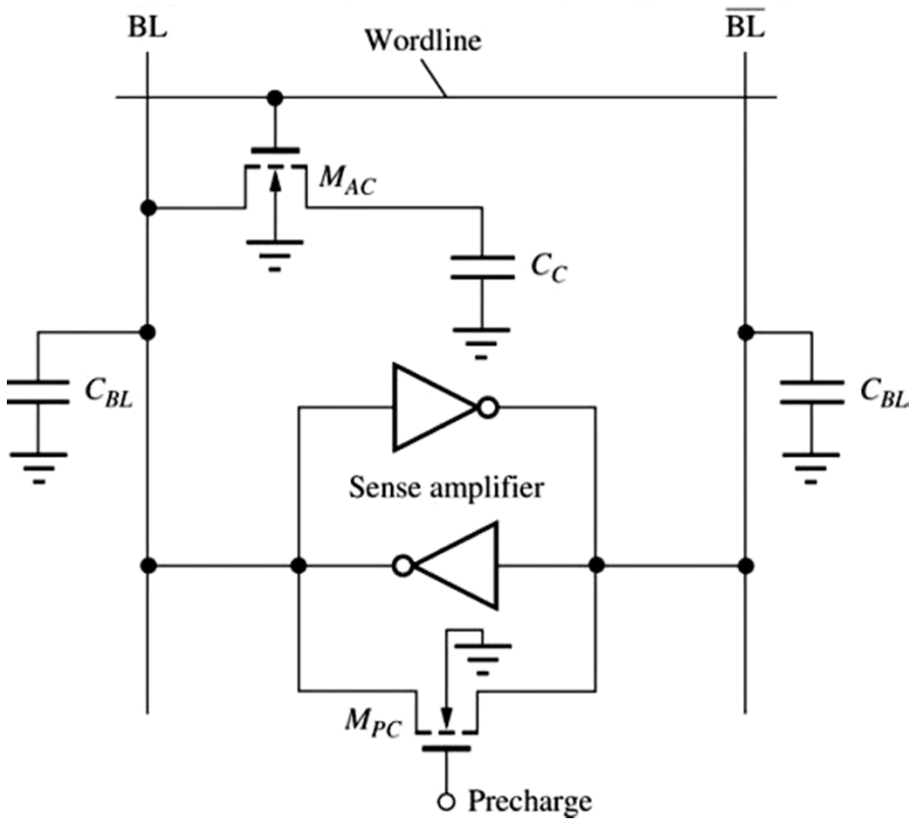
$$i_D = \frac{1}{2}\left(\frac{60\mu A}{V^2}\right)\left(\frac{2}{1}\right)(1.33-0.7)^2 = 23.6\mu A$$

- Note that the PMOS and NMOS drain currents are equal
- The power dissipation is given by:

$$P = 2i_D V_{DD} = 2(23.5\mu A)(3V) = 0.140mW$$

Sense Amplifiers

1-T Cell

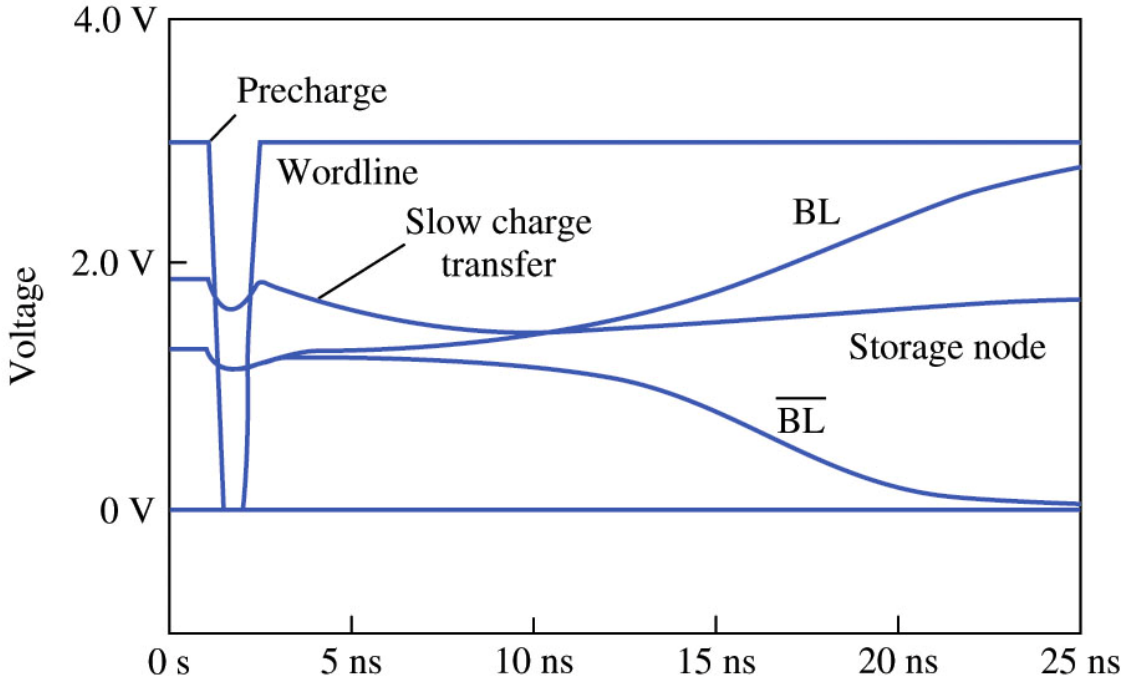


- The same sense amplifier used in the 6-T cell can be used for the 1-T cell in manner shown in the figure

Sense Amplifiers

1-T Cell

- The sense amplifier works the same as it did for the 6-T cell, but takes longer to reach steady state after precharge



Sense Amplifiers

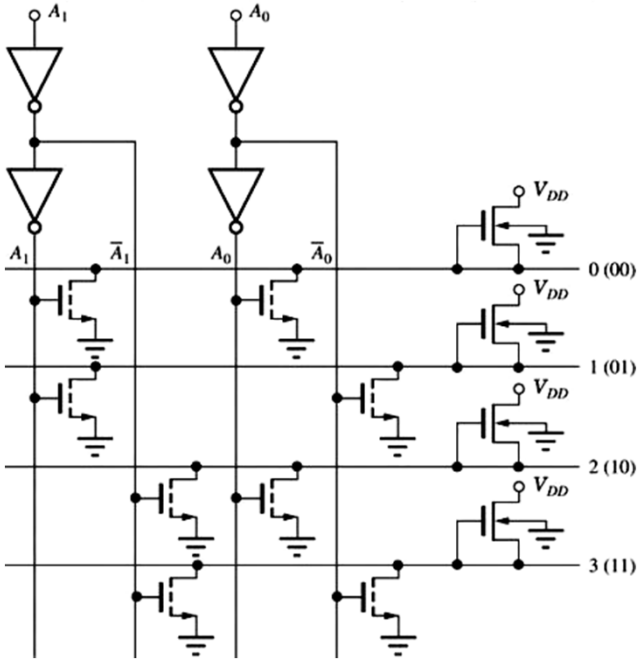
Boosted Wordline Circuit

- Obviously it is desired to have a fast access in many DRAM applications. By driving the wordline to a higher voltage (referred to as a boosted wordline), say 5V instead of 3V, it is possible to increase the amount of current supplied to the storage capacitors

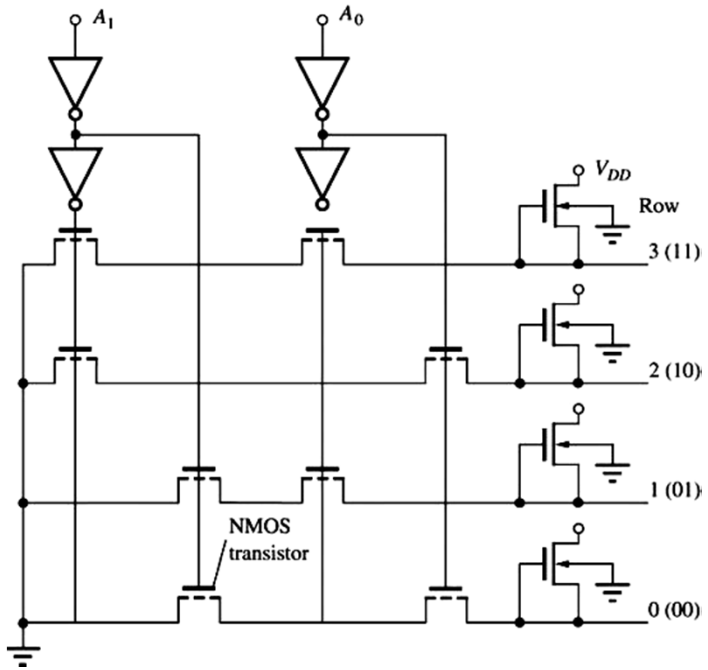
Address Decoders

NOR and NAND Decoders

- The following figures are examples of commonly used decoders for row and column address decoding



NMOS NOR Decoder



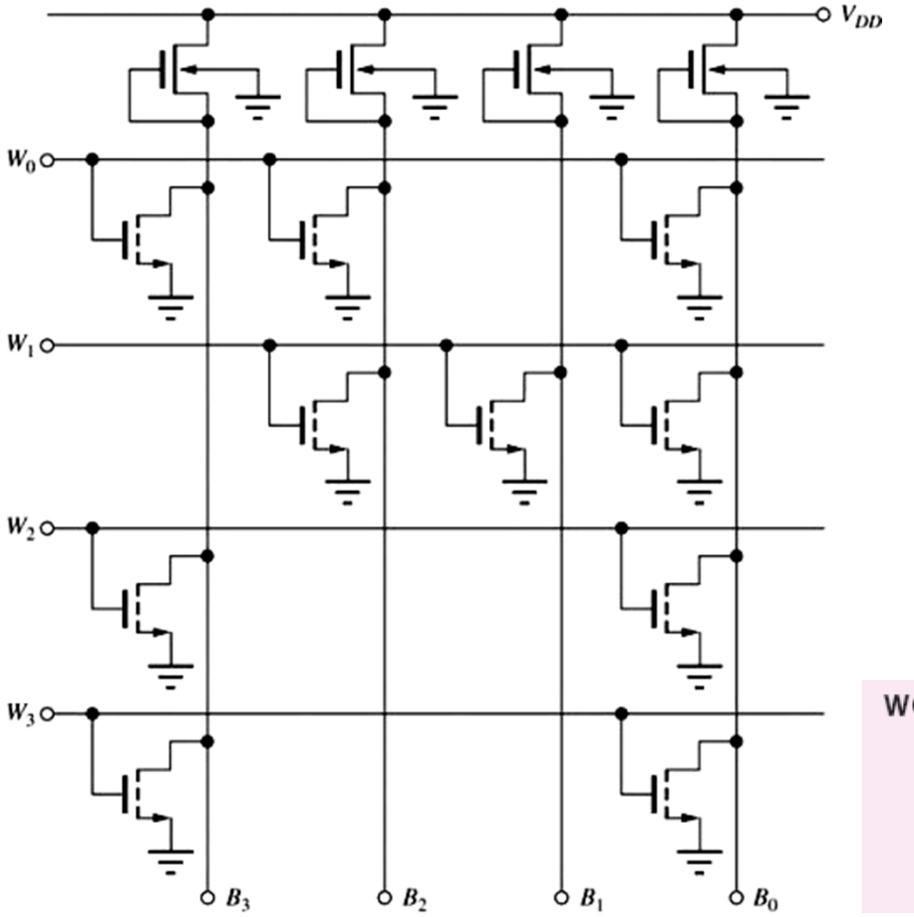
NMOS NAND Decoder

Read-Only Memory (ROM)

- ROM is often needed in digital systems such as:
  - Holding the instruction set for a microprocessor
  - Firmware
  - Calculator plug-in modules
  - Cartridge style video games

Read-Only Memory

NMOS NOR Array

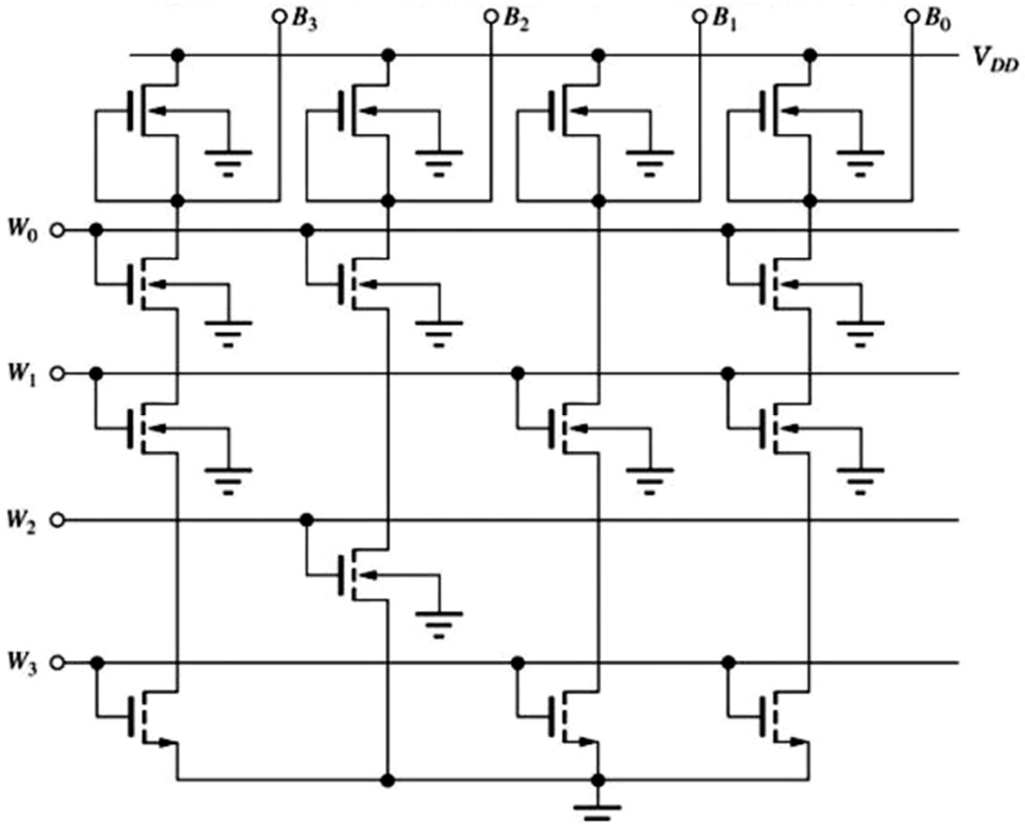


- The basic structure of the NMOS static ROM is shown in the figure
- The existence of an NMOS transistor means a "0" is stored at that address otherwise a "1" is stored
- Power dissipation is large

WORD	DATA
0	0010
1	1000
2	0110
3	0110

Read-Only Memory

NMOS NAND Array



- Another ROM option is the NAND array ROM which can be directly used with a NAND decoder

Programmable Read-Only Memory (PROM)

- The main problem with these previous ROMs is that they must be designed at the mask level, meaning that it is not a versatile product.
- To solve this problem, the programmable ROM (PROM) was introduced
- The standard PROM cannot be erased, so the erasable ROM (EPROM), and later, electrically erasable ROM (EEPROM) were introduced
- High density flash memories allow for electrical erasure and reprogramming of memory cells.
  - Use 2nd "floating" gate with stored charge to shift V_T.

RS Flip-Flops

Truth Tables

- The reset-set (RS) flip-flop can be easily realized by using either two cross-coupled NOR or NAND gates
- The RSFF has the following truth tables

NOR RSFF

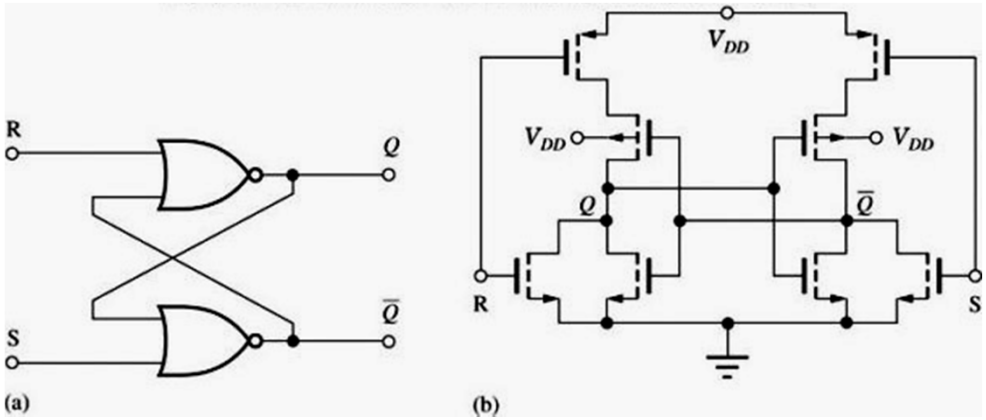
R	**S**	**Q**	$\overline{\mathbf{Q}}$
0	0	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
1	1	0	0

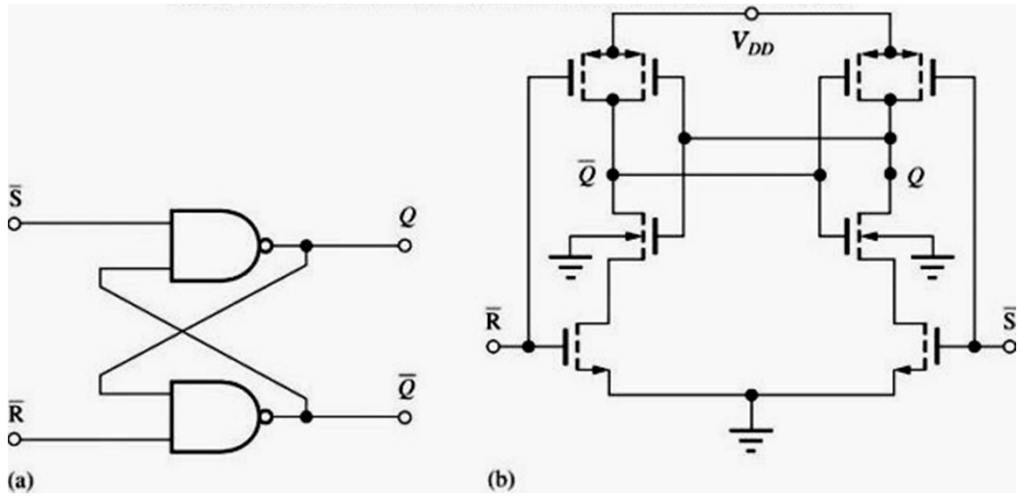
NAND RSFF

$\overline{\mathbf{R}}$	$\overline{\mathbf{S}}$	**Q**	$\overline{\mathbf{Q}}$
0	0	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
1	1	1	1

RS Flip-Flops

NOR and NAND Circuitry





NOR RS Flip-Flop

R	S	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
1	1	0	0

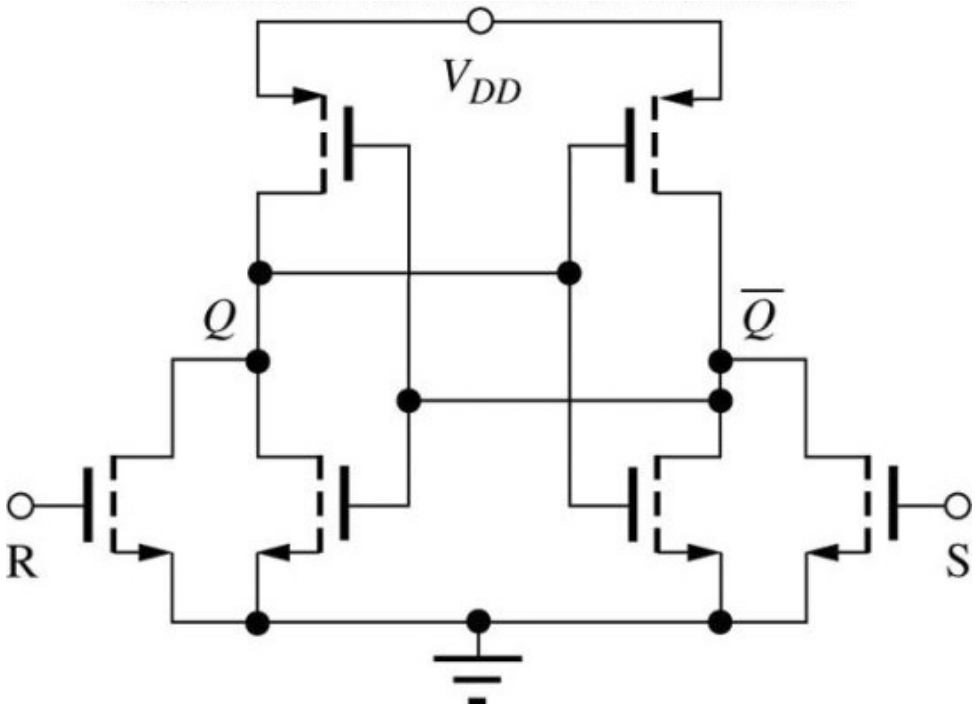
NAND RS Flip-Flop

$\overline{R}$	$\overline{S}$	Q	$\overline{Q}$
1	1	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
0	0	1	1

RS Flip-Flops

Simplified CMOS Circuit

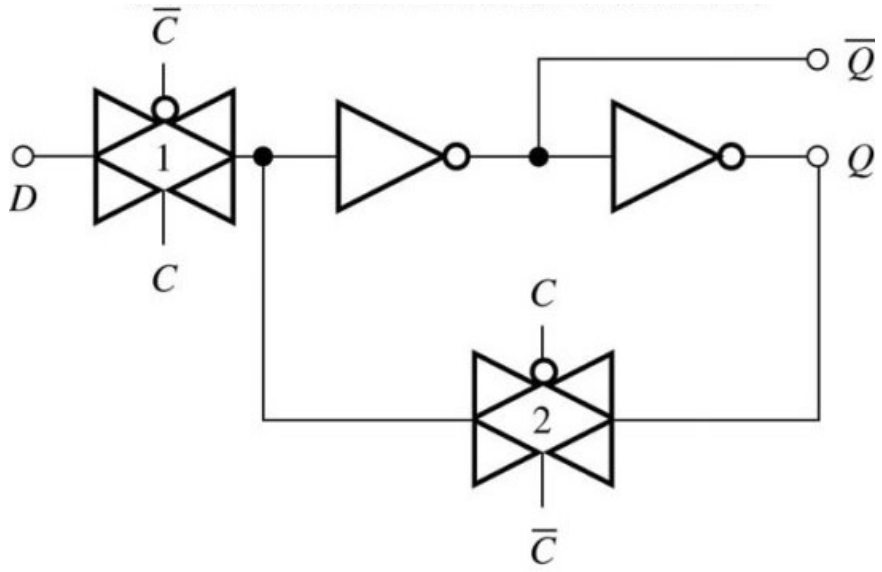
- Simplified RS flip-flop



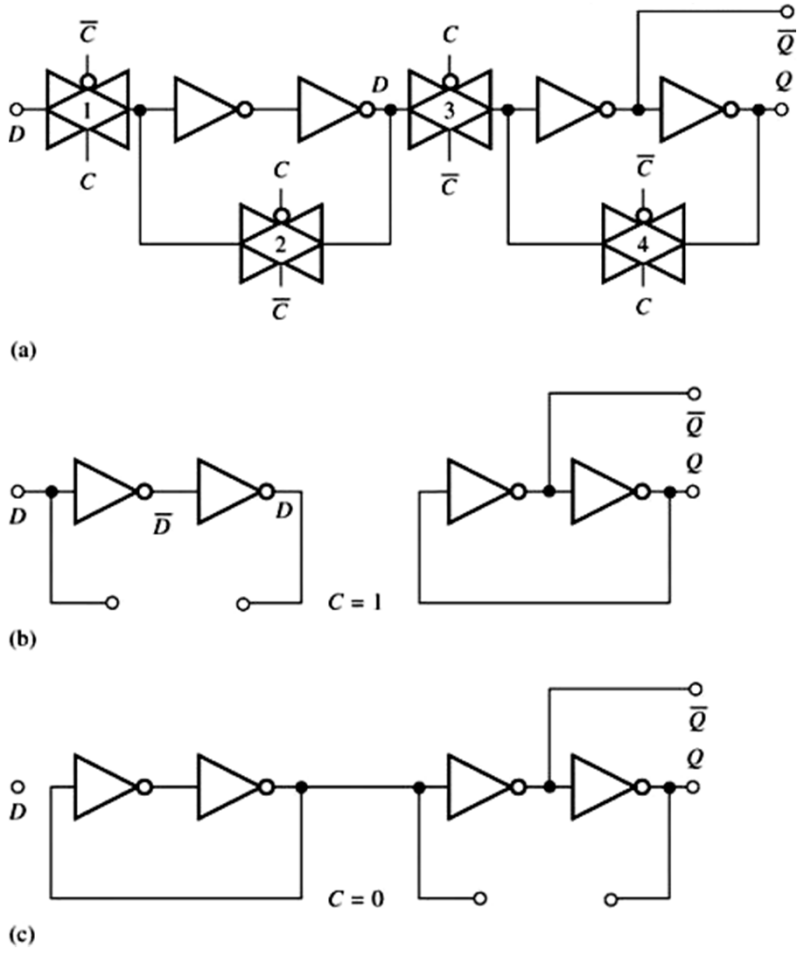
D-Latch

Transmission-Gate Implementation

- A very important circuit of digital systems is the D-Latch which is used for a D Flip-Flop
- Whenever clock C goes high in the D-Latch, the data on D is passed through to Q



Master Slave D Flip-Flop



- By using series D-Latches that latch the data on opposite clock phases, a master-slave D flip-flop can be realized

Scope of Finals Material

- Final will be comprehensive, but will emphasize material since Exam 2 (HW 7-9).
- Semiconductors: 2.1-2.10
- Diode Physics and Circuits: 3.1-3.18
- MOSFETs: 4.1-4.10
- MOS Logic Gates: 6.1-6.12
- CMOS Logic Gates: 7.1-7.7,7.9-7.10
- MOS Memory: 8.1-8.4

